

Lossless Broad-Band Monolithic Microwave Active Inductors

SHINJI HARA, MEMBER, IEEE, TSUNEO TOKUMITSU, MEMBER, IEEE,
AND MASAYOSHI AIKAWA, MEMBER, IEEE

Abstract—Lossless broad-band microwave active inductors for general-purpose use in microwave circuits are proposed and their characteristics are discussed. These active inductors are composed of a common-source cascode FET and a feedback FET, and operate in a wide frequency range with very low series resistance. A maximum Q factor of 65 is obtained. Theoretically, it can reach infinity. Furthermore, the inductance value can be controlled by an external voltage control.

I. INTRODUCTION

IN MMIC DESIGN, spiral inductors are often used to reduce chip size [1]–[3]. However, the area of a spiral inductor is still rather large compared to that of other lumped elements. It is also difficult to realize a broad-band spiral inductor, especially one of high inductance, because of stray capacitances. We previously proposed a microwave active inductor comprising a cascode FET and a feedback resistor for realizing wide-band MMIC's of smaller size [4]. It operates in a much higher frequency range than a spiral inductor. It is small and independent of the inductance value. However, because it includes an equivalent series resistance with a value approximately equal to the reciprocal of the GaAs FET transconductance, MMIC's where the active inductor can be applied are limited.

To overcome this limitation, we propose new types of microwave active inductors. One advantage of the newly proposed active inductors is low-loss or lossless characteristics due to the replacement of the feedback resistor by GaAs FET's, as well as the above-mentioned features realized in the previously proposed active inductor.

In this paper, further information on the previously proposed active inductor is given. The performance of the newly proposed active inductors is discussed and compared with the previously proposed active inductors and conventional spiral inductors.

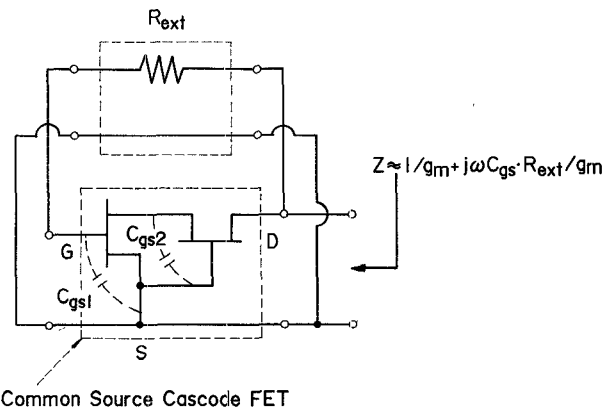


Fig. 1. Circuit configuration of the previously proposed active inductor.

II. PREVIOUSLY PROPOSED ACTIVE INDUCTOR

A. Configuration and Operation

The schematic of the previously proposed microwave active inductor is shown in Fig. 1 to explain the very high frequency operation of the active inductors. This active inductor is composed of a common-source cascode FET and a parallel feedback resistor (R_{ext}), where very high frequency operation is achieved by canceling the dominant parasitic capacitances in each FET of the cascode FET. When an FET is assumed to be the combination of only the transconductance g_m and the gate-source capacitance C_{gs} , the impedance Z of this active inductor is given by

$$Z = \frac{1 + j\omega C_{gs1} R_{ext}}{g_{m1} + j\omega \left[C_{gs1} - C_{gs2} \left(\frac{g_{m1}}{g_{m2}} \right) + \omega^2 C_{gs2} \left(\frac{C_{gs1} C_{gs2}}{g_{m2}^2} \right) \right]} \quad (1)$$

where the subscripts 1 and 2 correspond to the first and second FET, respectively, in the cascode FET. When the cascode FET is composed of the same FET's with the same g_m and C_{gs} , the gate-source capacitances C_{gs1} and C_{gs2} cancel each other. This is why this active inductor operates over a wide frequency range. Operation up to 10 GHz was confirmed through measurements [4]. The resonant frequency of these active inductors increases further as the FET's high-frequency characteristics improve. An

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S. Hara and T. Tokumitsu are with ATR Optical and Radio Communications Research Laboratories, Sanpeidani, Inuidani, Seika-cho, Sorakugun, Kyoto 619-01 Japan.

M. Aikawa was with ATR Optical and Radio Communications Research Laboratories, Kyoto, Japan. He is now with NTT Radio Communication Systems Laboratories, Kanagawa 238-03 Japan.

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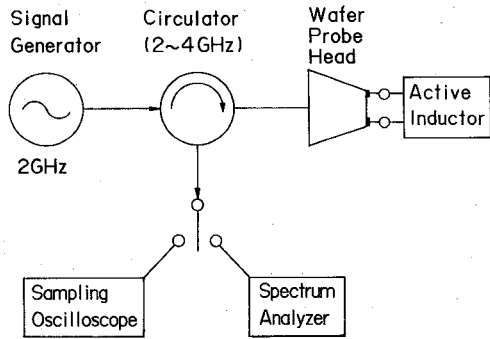


Fig. 2. Block diagram for distortion measurement of the active inductor.

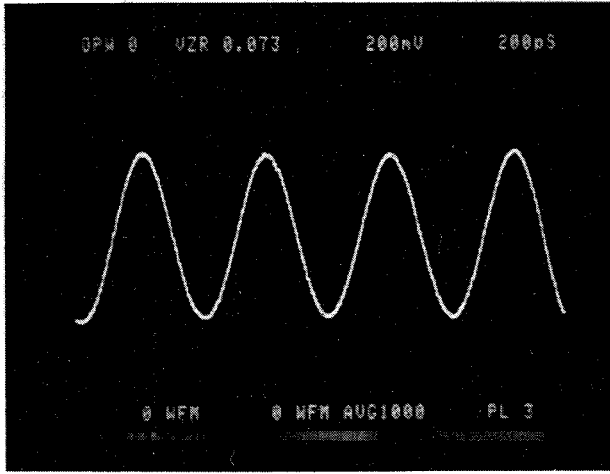


Fig. 3. Photograph of the waveform of the reflection signal.

equivalent circuit of this active inductor can be approximated by a resistor ($1/g_m$) and an inductor ($C_{gs}R_{ext}/g_m$) connected in series.

B. Linearity and Distortion

As a result of a simulation using commercially available nonlinear CAD software, it was concluded that the maximum handling power without distortion, P_{Lmax} , of the active inductor is represented as follows [5]:

$$P_{Lmax} = K/2 \times I_{dss} \times (V_{D2} - V_{G2}) \quad (2)$$

where I_{dss} is the saturation current of the FET, V_{D2} and V_{G2} are, respectively, the dc bias voltage of the drain and gate of the second FET in the cascode FET, and K is a coefficient, $2/3$ in this active inductor. When the input voltage is larger than $(V_{D2} - V_{G2})$, the gate voltage is larger than the drain voltage and the input current is distorted.

The test setup for measurement of linearity is shown in Fig. 2. A 2 GHz signal is injected into the active inductor through a circulator, and the reflected signal is observed by a spectrum analyzer and a sampling oscilloscope. Fig. 3 shows a photograph of the reflected signal waveform observed by the sampling oscilloscope when 10 dBm of power is injected into the active inductor with $2 \times 100 \mu\text{m}$ gate width FET's and a 1 k Ω feedback resistor. The waveform is not distorted. Here, the saturation current of

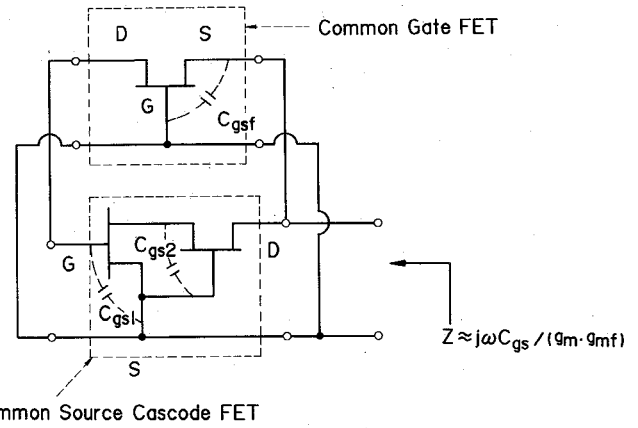


Fig. 4. Circuit configuration of the newly proposed active inductor. The feedback circuit is a common-gate FET.

the FET with a $100 \mu\text{m}$ gate width is about 13 mA. Thus, P_{Lmax} is predicted to be about 11 dBm from (2). Reflection versus incident power characteristics are linear up to 13 dBm incident power, but were not measured over 13 dBm incident power. The ratio of the second-harmonic power to the fundamental wave power of the reflected signal is 40 dB when the incident power is 0 dBm, and 23 dB when the incident power is 13 dBm. The dc power consumption of the measured active inductor is about 40 mW.

If FET's with double gate width are used, the active inductor can handle double power as shown in (2), and has $1/2$ series resistance because of double g_m . On the other hand, it consumes double dc power, needs a larger area, and has a lower resonant frequency because of the larger parasitic capacitances. However, the increase in chip size is not double but on the order of 20 to 30 percent, and the degradation of the resonant frequency is not 50 percent but 20 percent [4].

III. NEWLY PROPOSED ACTIVE INDUCTOR (TYPE (a))

A. Configuration and Operation

The schematic of the newly proposed active inductor is shown in Fig. 4. A common-gate FET is used in the feedback circuit instead of a resistor. The admittance Y of this active inductor is approximately represented by

$$Y = g_{mf} \left(1 - \frac{C_{gs2}g_{m1}}{C_{gs1}g_{m2}} \right) + \frac{g_{m1}g_{mf}}{j\omega C_{gs1}} \quad (3)$$

where the subscripts 1 and 2 correspond to the first and second FET in the common-source cascode FET, and the subscript f corresponds to the common-gate FET. When the common-source cascode FET is composed of the same FET's with the same g_m and C_{gs} , the conductance becomes zero in (3). As a result, this circuit functions as a lossless inductor whose impedance Z is represented by

$$Z = j\omega \frac{C_{gs}}{g_m g_{mf}} \quad (4)$$

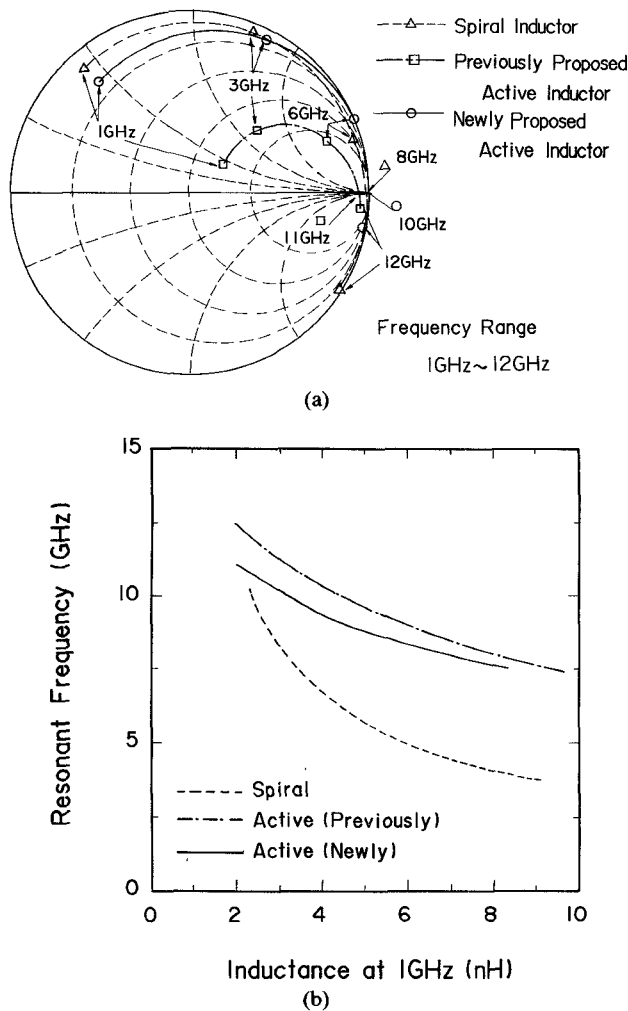


Fig. 5. Comparisons of the inductors. (a) Impedance. (b) Resonant frequency.

B. Calculated Performance

The characteristics of a conventional spiral inductor, the previously proposed active inductor, and the newly proposed active inductor are compared in Fig. 5. The broken line is for a spiral inductor, the chained-dotted line is for the previously proposed active inductor, and the solid line is for the newly proposed active inductor which includes a common-gate FET feedback circuit. The impedance characteristics are compared in Fig. 5(a). The value of each inductor is nearly 3.5 nH at 1 GHz. The spiral inductor is assumed to be fabricated on a 200- μm -thick GaAs substrate, and has a size of 300 μm \times 300 μm , a line width of 10 μm , and an Au line thickness of 2 μm . The active inductor characteristics are calculated using the parameters for a typical FET which has a cutoff frequency f_t of 20 GHz. The value of the feedback resistor or the gate width of a feedback FET is designed for an inductance value of 3.5 nH. The newly proposed active inductor has much lower loss characteristics than the previously proposed active inductor, and the series resistance values are nearly equal to that of the spiral inductor.

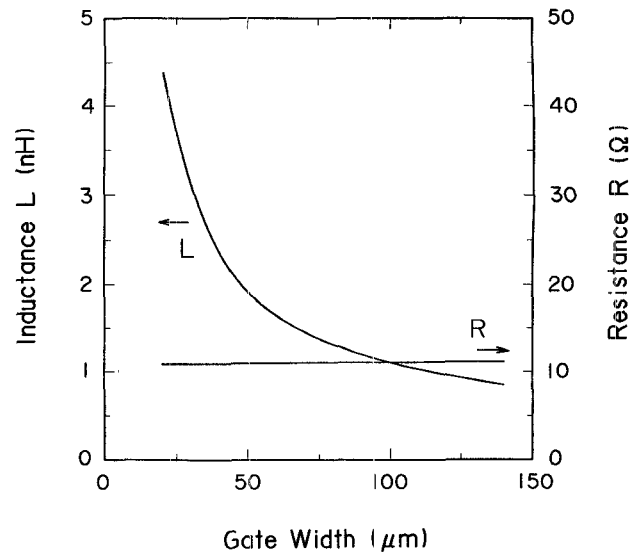


Fig. 6. Impedance at 1 GHz versus gate width of the feedback FET. Impedance is represented by series resistance and inductance.

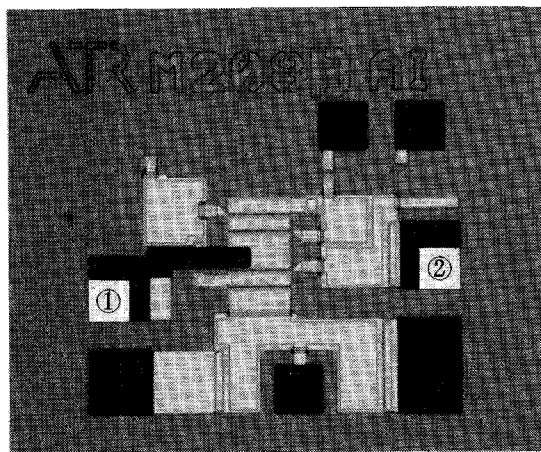
The resonant frequency, which is the maximum inductor operating frequency, is compared in Fig. 5(b) to the inductance value at 1 GHz. As shown in Fig. 5(b), the operating frequency range of the newly proposed active inductor is close to that of the previously proposed active inductor, and is higher than that of a spiral inductor, especially in the high inductance region. Furthermore, the operating frequency is extended as the FET's are improved [4].

Fig. 6 shows the impedance change caused by the gate width of the feedback FET, where the impedance is represented by series resistance and inductance, and the gate width of the common-source cascode FET is constant (100 μm). As shown in Fig. 6, the inductance value and the gate width are inversely proportional, which is implied in (4). The newly proposed active inductor also exhibits loss characteristics, because an actual FET has many parasitics not considered in the approximation used in (3) and (4). However, the loss is much lower than that of the previously proposed active inductor.

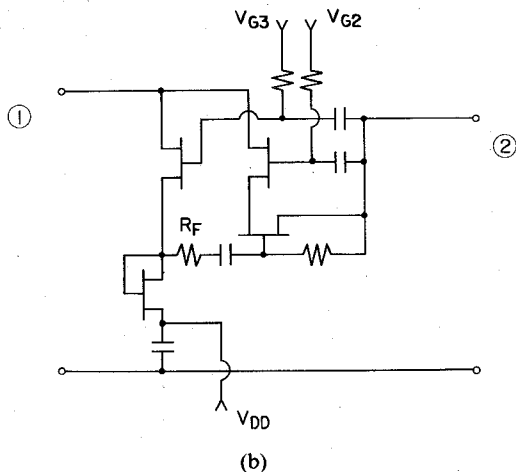
C. Experiment Result

A photograph of a fabricated GaAs monolithic active inductor and a circuit configuration diagram are shown in Fig. 7. Four 0.5 μm \times 100 μm single-gate ion-implanted FET's with a typical cutoff frequency of 20 GHz are employed. One FET is used for dc biasing. In the active inductor itself dc power consumption is about 70 mW. It is larger than that of the previously proposed active inductor, because the feedback element is not a resistor but an active device in the newly proposed active inductor. The power consumption of the FET feedback active inductor with higher inductance is lower, because a feedback FET with a smaller gate width is incorporated in it, as shown in Fig. 6.

The measured and the predicted impedance of the active inductor are shown in Fig. 8, where the port ② is grounded. The loss is slightly higher than the value pre-



(a)



(b)

Fig. 7. Schematics of the fabricated active inductor. (a) Photograph of the chip. (b) Circuit configuration.

dicted in Fig. 6. This is because the FET for dc bias does not offer infinite impedance for the active inductor. The Q value is about 2 at 3 GHz. A higher Q value can be obtained by using a FET with a wider gate as cascode FET.

D. Linearity and Distortion

As with the resistor feedback active inductor, the current is distorted when the input voltage is higher than $(V_{S3} - V_{G3})$, where V_{S3} and V_{G3} are the dc bias voltage of the source and gate of the feedback FET. Therefore, $P_{L\max}$ is predicted to be about 5 dBm when 100- μ m-gate-width FET's are used. Fig. 9 shows the reflection power versus incident power characteristics measured by the spectrum analyzer shown in Fig. 2. The circles represent the fundamental wave (2 GHz) and the triangles represent the second harmonics (4 GHz). The 1 dB compression point is about 5 dBm, which agrees with the predicted value. The handling power of the FET feedback active inductors which have same inductance is the same, because the inductance is determined by the gate width of the feedback FET in the FET feedback active inductor.

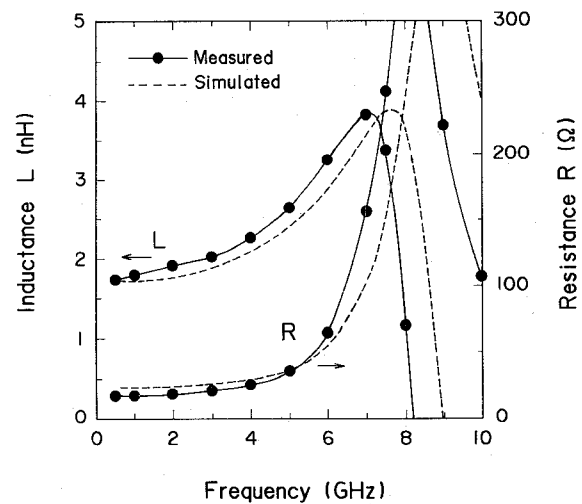


Fig. 8. Impedance-frequency characteristics of the CGF feedback active inductor. Impedance is represented by series resistance and inductance.

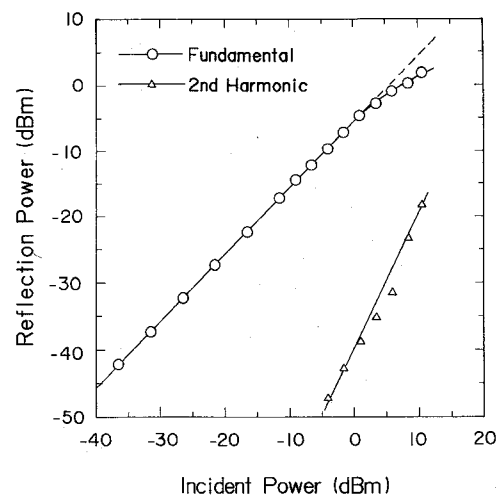


Fig. 9. Reflection power versus incident power of the active inductor.

IV. NEWLY PROPOSED ACTIVE INDUCTOR (TYPE (b))

A. Configuration and Operation

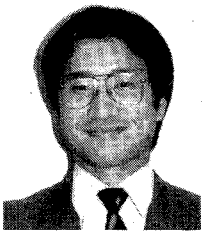
A schematic of the other type of active inductor is shown in Fig. 10. A common-gate cascode FET or a common-gate dual gate FET is used for the feedback circuit. In this case, the admittance Y of the parallel connection of a common-source cascode FET and a common-gate cascode FET is approximately expressed as follows:

$$Y = -g_m \frac{C_{gsf}}{C_{gs}} + \frac{1}{j\omega \left(\frac{C_{gs}}{g_m g_{mf}} \right)}. \quad (5)$$

Here, g_{mf} and C_{gsf} are, respectively, the transconductance and the gate-source capacitance of each FET in the common-gate cascode FET. Equation (5) shows that the equiv-

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Shinji Hara (M'88) was born in Toyama, Japan, in 1960. He received the B.E. and M.E. degrees in electronics engineering from Waseda University, Tokyo, Japan in 1982 and 1984, respectively.

In 1984, he joined Tokyo Research Laboratories of the Sharp Corporation, Chiba, Japan. Since September 1986, he has been a researcher at ATR Optical and Radio Communications Research Laboratories, Osaka, Japan, on leave from the Sharp Corporation. At ATR, he has been

engaged in research on circuit design technologies to realize highly integrated MMIC's.

Mr. Hara is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information and Communication Engineers of Japan.



Tsuneo Tokumitsu (M'88) was born in Hiroshima, Japan, in 1952. He received the B.S. and M.S. degrees in electronics engineering from Hiroshima University, Hiroshima, in 1974 and 1976, respectively.

He joined the Yokosuka Electrical Communication Laboratories, Nippon Telegraph and Telephone Public Corporation, Yokosuka, in 1976, where he did research on microwave and millimeter-wave integrated circuits, MIC's, and MMIC's and worked on the development of onboard satellite equipment. In September 1986, he joined ATR Optical and Radio Communications Research Laboratories, Osaka, where he is currently engaged in research on highly integrated MMIC's for future digital mobile communications.

Mr. Tokumitsu is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Masayoshi Aikawa (M'78) was born in Saga, Japan, on October 16, 1946. He received the B.S., M.S., and Dr. Eng. degrees in electronics engineering from Kyushu University, Fukuoka, Japan, in 1969, 1971, and 1985, respectively.

In 1971, he joined the Musashino Electrical Communication Laboratories, Nippon Telegraph and Telephone Public Corporation, Tokyo, Japan, where he did research and development work on microwave and millimeter-wave integrated circuits, MIC's, MMIC's, and equipment for 20 GHz digital radio trunk transmission systems and 26 GHz subscriber radio systems. In 1986, he joined ATR Optical and Radio Communications Research Laboratories, Osaka, Japan, where he was engaged in research on basic techniques for future digital mobile communications. He is now with the NTT Radio Communication Systems Laboratories, Yokosuka, where he has been engaged in research and development work on monolithic microwave and millimeter-wave integrated circuits and their applications.

Dr. Aikawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan.